HIGH-TEMPERATURE ISOLATED TWO-CHANNEL TRANSCEIVER

FEATURES

- ▲ Supply voltage 4.5…5.5V.
- ▲ Dual Transmitter/Receiver (TX/RX) channels.
- ▲ Operating junction temperature from -60°C to +230°C.
- ▲ Data rate up to 2 Mbits/second per channel.
- ▲ Transient common mode current immunity of 100mA (50kV/µs across 2pF of inter-winding capacitance).
- ▲ Hysteresis on digital input for noise immunity.
- ▲ Enable control signal on both TX and RX functions.
- ▲ OOK (On-Off Keying) modulation.
- ▲ 3 bits programmable carrier frequency for EMC compliance.
- ▲ Configurable TX and RX modulation polarity.
- ▲ Latch-up free.
- ▲ Ruggedized SMT packages (CSOIC28).
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Intelligent Power Modules (IPM).
- ▲ Power conversion, power generation and motor drive in aeronautics.
- ▲ Isolated gate drive for IGBT, MOSFET, JFET and SiC Transistors
- ▲ Isolated sensor interfaces.
- ▲ Isolated power inverters.

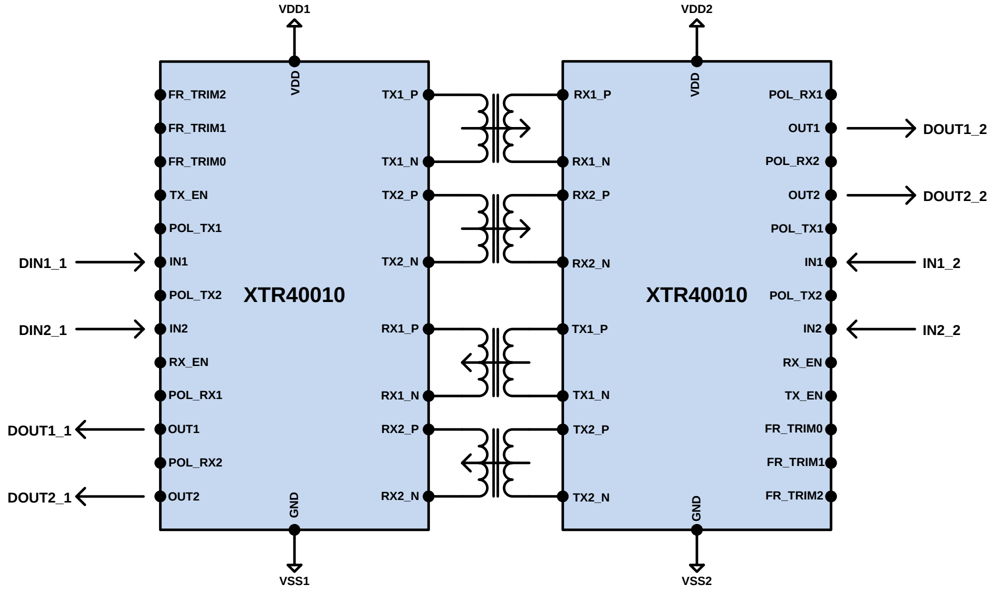
DESCRIPTION

The XTR40010 implements a high-temperature dual-channel (2 TX/RX) isolated data transceiver. It can be used as general purpose isolated transceiver. It is also well suited for isolated data communication between a microcontroller or a PWM controller, with the intelligent power gate driver XTR26010. The galvanic isolation is achieved by external high-temperature 1:1 pulse transformers.

The XTR40010 integrates in a single package 2 transceivers (two full duplex channels). The implementation of 2 full duplex TX/RX isolated channels requires 2 XTR40010, one being connected to one side of the transformers and one to the other side. When used with XTR26010, the XTR40010 allows implementing a 2 full duplex TX/RX channels with only one instance of XTR26010. Indeed, the XTR26010 transceiver is fully compatible with the XTR40010. The complete solution is optimized to minimize the size of the transformer, the number of external components, the transmission delay (<120ns) and to maximize the noise margin, even in harsh dV/dt conditions (50kV/µs across 2pF of inter-winding capacitance).

PRODUCT HIGHLIGHT

Dual full duplex TX/RX channels



ORDERING INFORMATION

X	TR	40	010
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel; R = HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR40010-BD	-60°C to +230°C	Bare die		XTR40010
XTR40011-S	-60°C to +230°C	Ceramic SOIC	28	XTR40011
XTR40011-D	-60°C to +230°C	Ceramic side braze DIP	28	XTR40011
XTR40012-S	-60°C to +230°C	Ceramic SOIC	16	XTR40012

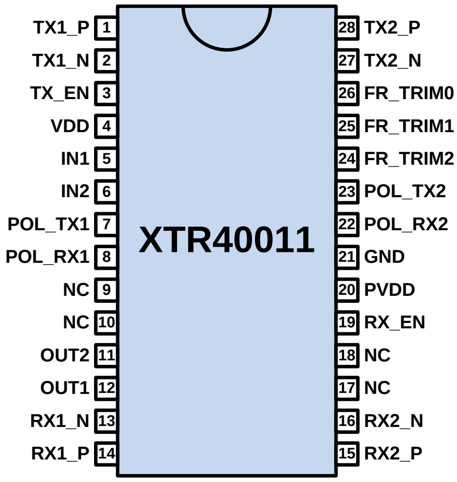
Other packages and packaging configurations possible upon request.

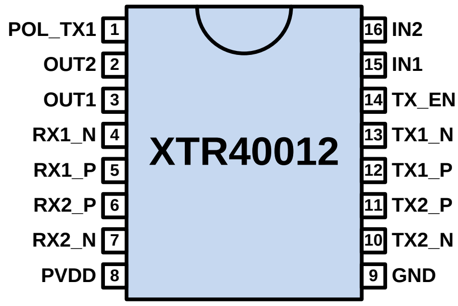
ABSOLUTE MAXIMUM RATINGS

Voltage between PVDD and GND	-0.5 to 6V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

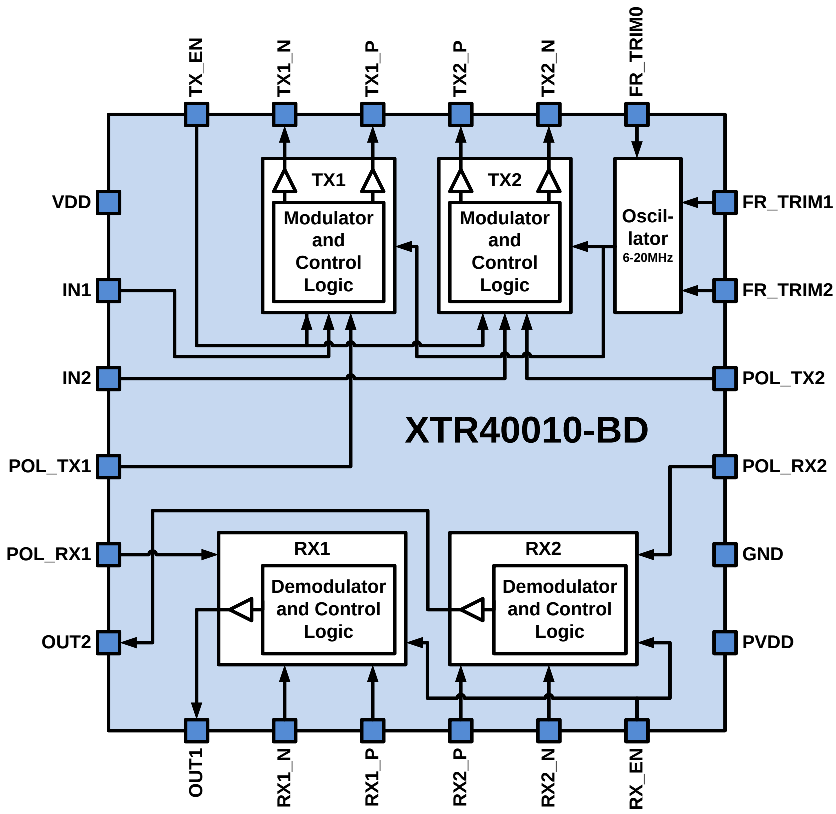
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PACKAGING





BLOCK DIAGRAM (XTR40010-BD)



Die level block diagram showing all available functionalities and bond-pads.

PIN DESCRIPTION (CSOIC28)

Pin number	Name	Description
1	**TX1_P**	Positive differential output of the transmitter TX1. To be connected to the primary of the pulse transformer.
2	**TX1_N**	Negative differential output of the transmitter TX1. To be connected to the primary of the pulse transformer.
3	**TX_EN**	Digital input transmitter enable pin to be connected to **PVDD** to enable TX1 and TX2.
4	**VDD**	For proper operation this pin must be connected to **PVDD**.
5	**IN1**	Schmitt-triggered digital input of transmitter TX1.
6	**IN2**	Schmitt-triggered digital input of transmitter TX2.
7	**POL_TX1**	Schmitt-triggered digital input that sets the polarity of the transmitter TX1. To be connected to **GND** for non-inverting input or to **PVDD** for inverting input.
8	**POL_RX1**	Schmitt-triggered digital input that sets the polarity of the receiver RX1. To be connected to **GND** for non-inverting output or to **PVDD** for inverting output.
9	**NC**	Do not connect.
10	**NC**	Do not connect.
11	**OUT2**	Digital output of receiver RX2.
12	**OUT1**	Digital output of receiver RX1
13	**RX1_N**	Negative differential input of receiver RX2. To be connected to the secondary of the pulse transformer.
14	**RX1_P**	Positive differential input of receiver RX2. To be connected to the secondary of the pulse transformer.
15	**RX2_P**	Positive differential output of receiver RX2. To be connected to the secondary of the pulse transformer.
16	**RX2_N**	Negative differential output of receiver RX2. To be connected to the secondary of the pulse transformer.
17	**NC**	Do not connect.
18	**NC**	Do not connect.
19	**RX_EN**	Schmitt-triggered digital input enable pin for the receivers. To be connected to **PVDD** to enable RX1 and RX2.
20	**PVDD**	Positive power supply supplying all the circuit.
21	**GND**	Negative power supply supplying all the circuit.
22	**POL_RX2**	Schmitt-triggered digital input that sets the polarity of the receiver RX2. To be connected to **GND** for non-inverting output or to **PVDD** for inverting output.
23	**POL_TX2**	Schmitt-triggered digital input sets the polarity of the transmitter TX2. To be connected to **GND** for non-inverting input or to **PVDD** for inverting input.
24	**FR_TRIM2**	Schmitt-triggered digital input control bits for oscillator frequency configuration (MSB=**FR_TRIM2**, LSB=**FR_TRIM0**).
25	**FR_TRIM1**	
26	**FR_TRIM0**	
27	**TX2_N**	Negative differential output of transmitter TX2. To be connected to the primary of the pulse transformer.
28	**TX2_P**	Positive differential output of transmitter TX2. To be connected to the primary of the pulse transformer.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **PVDD-GND**	4.5		5.5	V
Voltage on all other pins[1]	GND-0.3		PVDD	V
Operating Frequency **FR**		6-20		MHz
Junction Temperature[2] $\mathbf{T_j}$	-60		230	°C

[1] During transient operation, TX1_P/N, TX2_P/N and RX1_P/N, RX2_P/N can reach values under 0V and above VDD. Extreme values are limited by internal clamping diodes to GND and to VDD.
[2] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for VDD-GND=5V and T_j=25°C.

Parameter	Condition	Min	Typ	Max	Units
Supply voltage					
VDD-GND		4.5		5.5	V
Supply current (2 TX/RX channel)					
Duty cycle=0%	INx="0", C_{OUT}=50pF, FR_TRIM="000", POL_xxx="0"		1		mA
Duty cycle=50%	INx=1MHz, C_{OUTx}=50pF, FR_TRIM="000", POL_xxx="0"		8		mA
Duty cycle=100%	INx="1", C_{OUT}=50pF, FR_TRIM="000", POL_xxx="0"		18		mA
Quiescent curent	TX_EN="0" and RX_EN="0"		100		µA
Dynamic specifications					
Maximum data rate	FR_TRIM<2:0> = “000”			2	Mbps
Modulation frequency	Using FR_TRIM<2:0> control signals		6-20		MHz
Modulation frequency variation		-30		+30	%
Modulation frequency duty cycle		48.5		51.5	%
Propagation delay	FR_TRIM<2:0> = “0xx”		120		ns
Jitter (RMS cycle-2-cycle)			±25		ns
Start-up time	When xx_EN goes to “1”		100		ns
Isolation performances (using appropriate pulse transformer as described in AN-00371-13)					
DC isolation (only depends on the pulse transformer)	At 2500V		10		MΩ
Transient common mode current immunity $\mathbf{I_{CM}}$	dV/dt [kV/µs]=I_{CM} [mA]/C_{ww} [pF]			100	mA
TX Channel					
Driver output ON/OFF resistance	On each TX output		10		Ω
$\mathbf{V_{IH}}$ of digital inputs		3.84			V
$\mathbf{V_{IL}}$ of digital inputs				1.1	
Hysteresis		1.6	2	2.4	
RX Channel					
$\mathbf{V_{OH}}$ of digital outputs	I_{OUT}=8mA	4.4			V
$\mathbf{V_{OL}}$ of digital outputs	I_{OUT}=8mA			0.63	V

THEORY OF OPERATION

Introduction

The XTR40010 implements a dual-channel isolated data transceiver. It can be used in any application where there is a need to galvanically isolate a digital data line. The galvanic isolation is achieved by an external magnetic transformer for each digital signal. The XTR40010 integrates in a single package 2 transceivers (2 TX/RX channels).
The implementation of 2 isolated full duplex TX/RX channels requires 2 XTR40010, one being connected to the primary side of the transformers and the other to the secondary side.
The XTR40010 contains 2 identical transmitters and 2 identical receivers. In the following sections, only one transmitter and one receiver will be described, and thus, the pin index 1,2 will be omitted for simplicity.

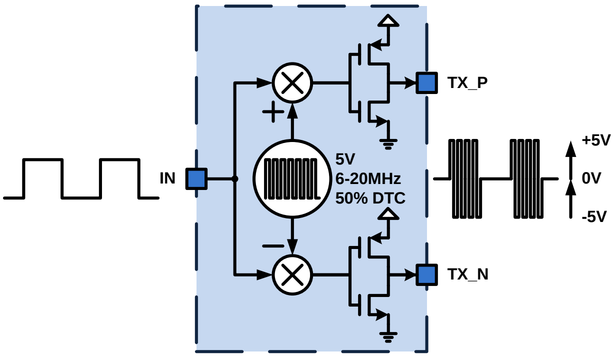
Transmitter operation

The transmitter is composed of the following functions (as shown in the figure below):

- Oscillator: This block generates a clock with a 3-bits programmable frequency using the **FR_TRIM<2:0>** pins. This can be used to tune the carrier frequency to avoid EMC issues. The following table shows the typical frequency values that can be obtained:

FR_TRIM<2:0>	Carrier Frequency [MHz]
000	20
001	17.5
010	15
011	12.5
100	10
101	8.75
110	7.5
111	6.25

- Modulator: This block implements a classical On-Off Keying (OOK) modulation using the clock generated by the oscillator and the digital input signal. If **POL_TX** pin is set to "0", a digital "1" at the input **IN** of the transmitter will be transferred as a differential ±5V at the output pins **TX_P/TX_N**. On the other hand, a digital "0" is transferred as a 0V versus **GND** at the output pins **TX_P/TX_N** of the transmitter. Depending on the application at system level, this behavior can be inverted by setting **POL_TX** to "1".
- The output buffer: It consists of several inverters with a typical R_{ON} of 10Ω for the last stage (NMOS or PMOS). This buffer is driven by two complementary signals generated by the modulator. These signals have a duty cycle very close to 50% to guarantee no DC current in the primary inductance of the pulse transformer. This DC current can induce a magnetic field that could saturate the magnetic core and compromise the data transfer.

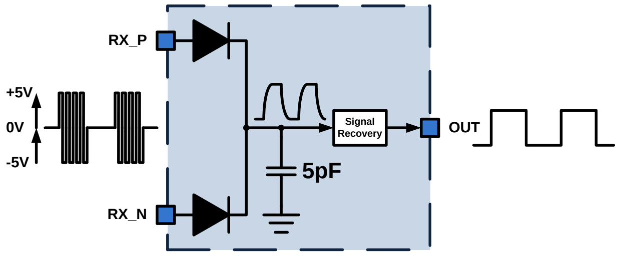


Transmitter truth table

EN_TX	POL_TX	IN	TX_P	TX_N
0	x	x	0	0
1	0	0	0	0
1	0	1	CK	/CK
1	1	0	CK	/CK
1	1	1	0	0

Receiver operation

The receiver implements a classical full-wave rectification to demodulate the signal received on the pulse transformer secondary winding (as shown in the figure below). The signal recovery block aims to ensure immunity versus possible high dv/dt, which induces common mode current from one side of the pulse transformer to the other side. This common mode current can induce errors in the data transmission from the transmitter side to the receiver side. When a dv/dt event happens, it is detected by this block. During the dv/dt event the output data is kept at its value just before the dv/dt event. After the dv/dt event, the input data is transferred to the output.



Receiver truth table

EN_RX	POL_RX	RX_P	RX_N	OUT
0	x	x	x	0
1	0	0	0	0
1	0	CK	/CK	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	**forbidden**
1	1	0	0	1
1	1	CK	/CK	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	**forbidden**

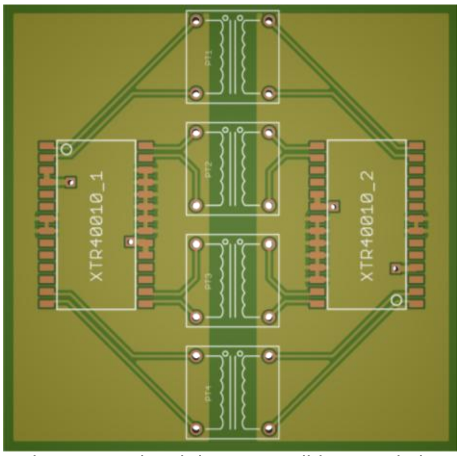
Pulse transformer

The pulse transformer specifications and design guidelines are given in the application note "Pulse Transformer Design Guidelines" (AN-00371-13).

TX/RX routing guidelines

As the TX/RX signals are clocked at 20MHz with sharp transitions, a special care must be taken for their routing to and from the pulse transformers. If no care is taken for their routing, a strong coupling between different TX or RX signals may affect dV/dt immunity. It is also recommended to keep enough distance between the pulse transformers to avoid coupling between neighbors. Indeed, if the RX input traces have asymmetrical parasitic coupling capacitances to noisy traces in addition to a dV/dt event, a voltage difference can appear between RX inputs leading to a possible false transient state. It is also recommended to keep enough distance between the pulse transformers to avoid magnetic coupling between neighboring magnetic cores.

An example of good practice for a PBC routing between two XTR40010 is given hereafter:

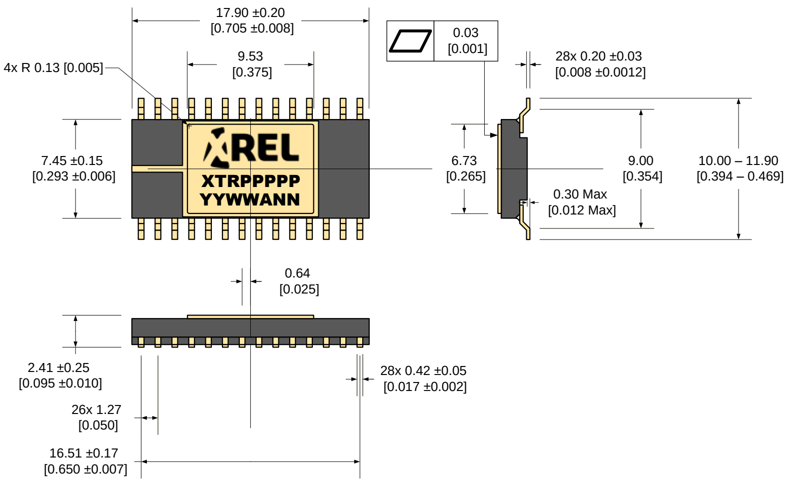


If for any other constraints it is not possible to optimize the routing as indicated above, it is recommended to add pull-down resistors to **VSS** in the range of 1kΩ to 10kΩ on each input of the RX and a capacitor in the range of 5pF to 10pF between differential RX inputs.

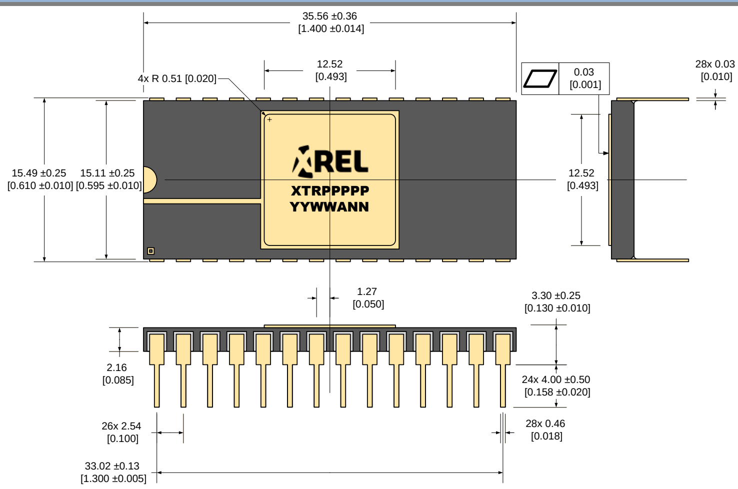
PACKAGE OUTLINES

Dimensions shown in mm [inches].

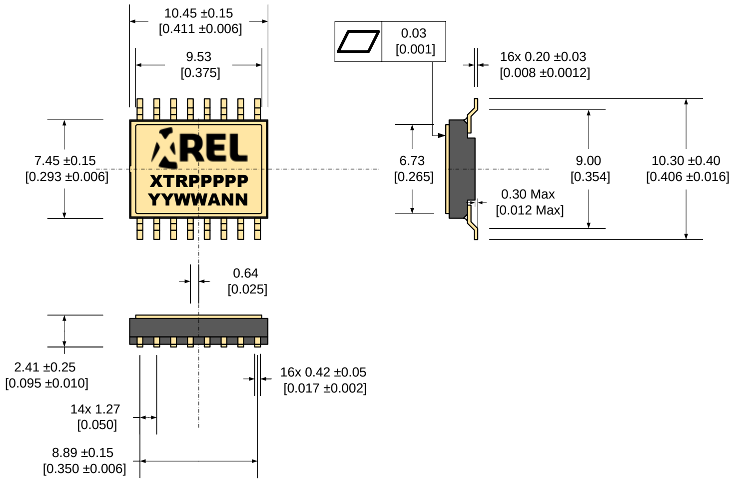
Ceramic Small Outline IC SOIC28



Ceramic Side Brazed Dual In-line DIP28



Ceramic Small Outline IC SOIC16



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- ✓ Information: info@x-relsemi.com
- ✓ Support: support@x-relsemi.com

X-REL Semiconductor
90, Avenue Léon Blum
38100 Grenoble
France