

# HIGH-TEMPERATURE, 300V LOW-SIDE POWER CASCODE TRANSISTOR WITH DRIVER

## FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Robust operation as low-side switch with drain spikes up to 650V.
- ▲ Standard Schmitt-trigger CMOS input
- ▲ Exists in inverting and non-inverting versions (upon request).
- ▲ Plug-and-play with any digital 5V output.
- ▲ Over current (desaturation) protection with soft turn-off.
- ▲ Under voltage lockout UVLO protection (MOSFET OFF).
- ▲ Low on-resistance : 650 mΩ @ 230°C
- ▲ Large peak current capabilities: 8.3A @ 230°C
- ▲ Low On- and Off-time (220nsec and 290nsec @ 230°C).
- ▲ Latch-up free.
- ▲ Ruggedized 8-lead tabless TO254 package.

## APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ DC/DC converters, motor drive, switching power supplies, switching control.

## DESCRIPTION

XTR23012 features a 300V power cascode transistor with integrated driver designed for extreme reliability and high temperature applications such as DC/DC converters, motor control and power switching. XTR23012 parts are intended to be used as low side switches. They can sustain drain spikes up to 650V. XTR23012 parts can be directly driven by any 5V digital output, making them fully plug-and-play devices, avoiding any time consuming optimization of the matching network between driver and power transistor.

XTR23012 parts are robust to usual spikes associated with parasitic inductors and fast transients in switching applications.

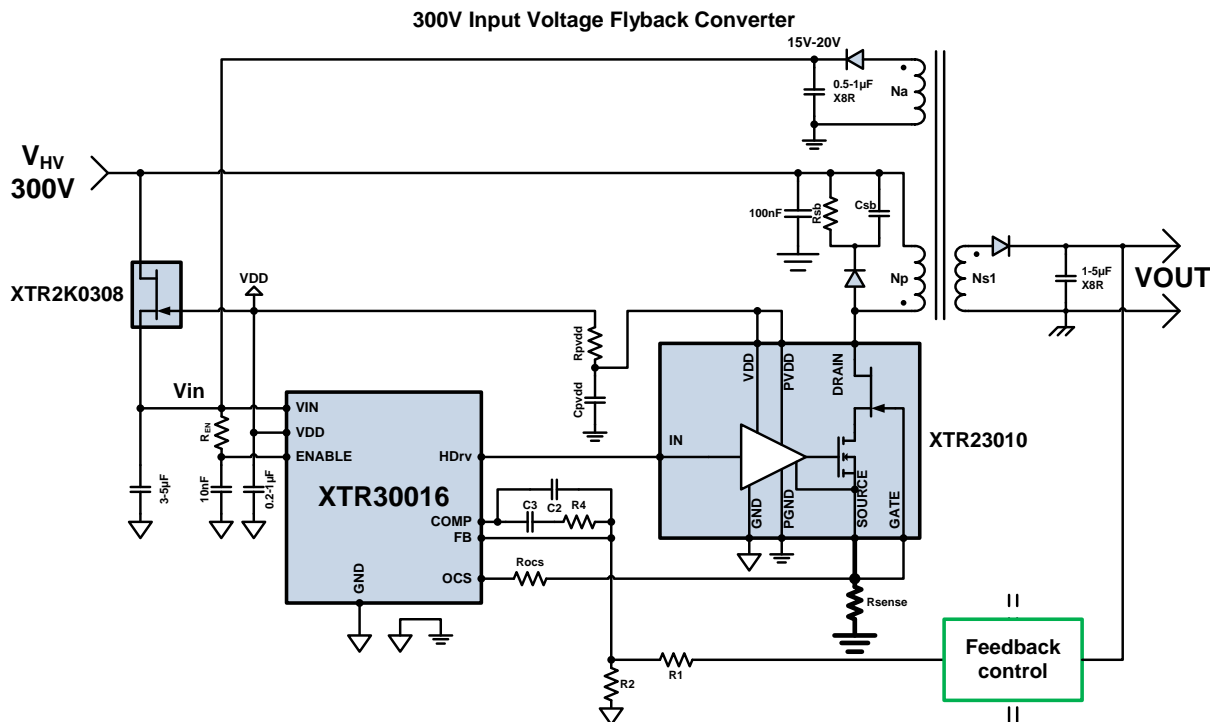
Features of XTR23012 family parts include UVLO (driver state is OFF whenever the supply is too low), desaturation protection of the output transistor with soft shut-down functionality and possibility to select inversion of control signal (upon request).

Full functionality is guaranteed from -60°C to +230°C, though operation well beyond this temperature range is achieved.

The XTR23012 has been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

The XTR23012 is available in ruggedized 8-lead tabless TO254 packages. Ask X-REL Semiconductor for other packages and bare die availability.

## PRODUCT HIGHLIGHT



## ORDERING INFORMATION

<p>X</p> <p>↓</p> <p>Source:</p> <p>X = X-REL Semi</p>	<p>TR</p> <p>↓</p> <p>Process:</p> <p>TR = HiTemp, HiRel</p> <p>R = HiRel</p>	<p>23</p> <p>↓</p> <p>Part family</p>	<p>012</p> <p>↓</p> <p>Part number</p>
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Product Reference	Temperature Range	Package	Pin Count	Marking
XTR23012-T	-60°C to +230°C	Tabless TO254	8	XTR23012

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply. Ask X-REL Semiconductor for bare die availability.

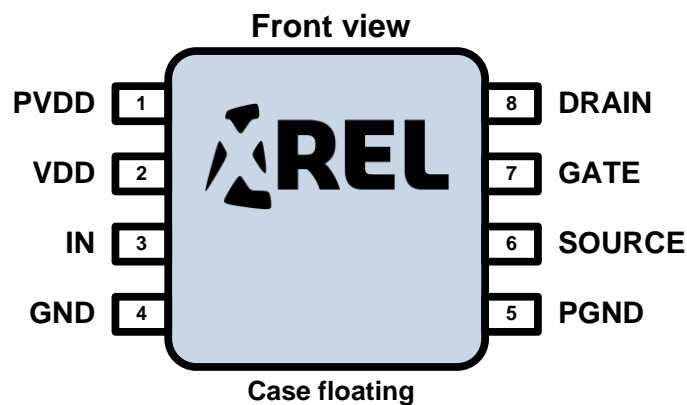
## ABSOLUTE MAXIMUM RATINGS

Voltage on DRAIN to SOURCE	-1.5 to 650V
Voltage on IN and VDD to GND	-0.5 to 6.0V
Voltage on PVDD to PGND	-0.5 to 7.5V
Voltage on SOURCE to PGND	-1 to 1V
Voltage on PVDD to VDD	-0.5 to 50V
Voltage on PGND to GND	-0.5 to 50V
Storage temperature range	-70°C to +230°C
Operating junction temperature range	-70°C to +250°C
ESD classification	1kV HBM MIL-STD-883

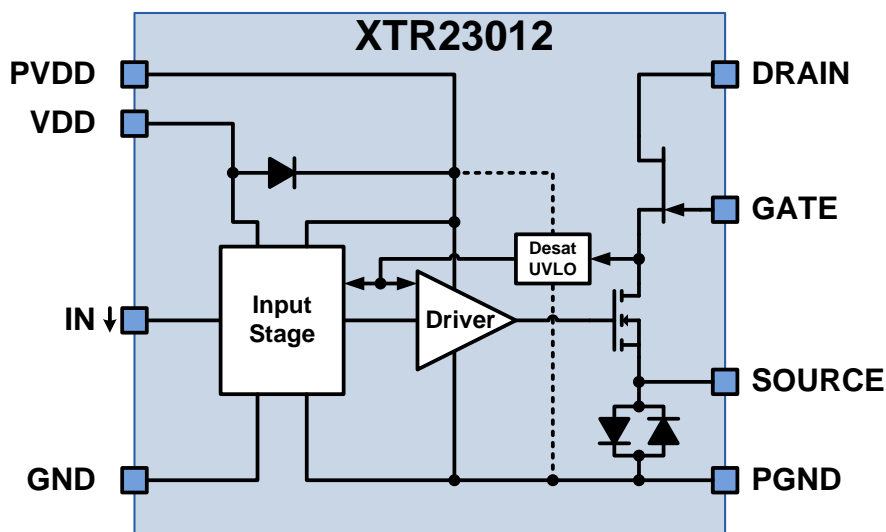
**Caution:** Stresses beyond those listed in “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may permanently affect device reliability.

## PACKAGING

### Tabless TO254



## BLOCK DIAGRAM



Arrows aside pin names indicate whether the input is internally pulled up or down.

**PIN DESCRIPTION**

XTR23012-T		
Pin Number	Name	Description
1	PVDD	Supply voltage of power section. Referenced to PGND.
2	VDD	Supply voltage of the input section. Referenced to GND.
3	IN	High-side input signal. Referenced to GND. <u>Internally pulled down.</u>
4	GND	Circuit ground.
5	PGND	Ground of the power stage.
6	SOURCE	Source of the power NMOS transistor.
7	GATE	Gate of the cascode transistor. In some cases it is recommended to connect a resistor 10-20 Ohm from GATE to SOURCE to avoid ringing during turn-on or turn-off
8	DRAIN	Drain of the equivalent power transistor.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Min	Typ	Max	Units
Supply voltage VDD to GND $V_{DD}$	4.5		5.5	V
Supply voltage PVDD to PGND $V_{PVDD}$	See UVLO threshold		5.5	V
DRAIN-SOURCE voltage $V_{DS}$	-1		300	V
Input voltage on IN to GND $V_{IN}$	-0.3		VDD	V
PVDD to VDD voltage <sup>1</sup>	-1		40	V
PGND to GND voltage	-1		40	V
SOURCE to PGND voltage	-0.7		0.7	V
Junction Temperature <sup>2</sup> $T_j$	-60		230	°C

<sup>1</sup> A diode connected from VDD (anode) to PVDD (cathode) exists. This diode may be used as bootstrap diode in floating driver applications.

<sup>2</sup> Operation beyond the specified temperature range is achieved with little degradation on electrical parameters.

**THERMAL CHARACTERISTICS**

Parameter	Condition	Min	Typ	Max	Units
<b>XTR23012-T (8-lead TO254)</b>					
Thermal Resistance: J-C $R_{Th\_J-C}$			5		°C/W
Thermal Resistance: J-A $R_{Th\_J-A}$			45		°C/W

**ELECTRICAL SPECIFICATIONS**
**STATIC CHARACTERISTICS**

 Unless otherwise stated, VDD=PVDD=5V, GND=PGND=SOURCE, IN=0V, I<sub>DRAIN</sub>=1A, -60°C<T<sub>C</sub><230°C.

Parameter	Condition	Min	Typ	Max	Units
<b>Supply Current</b>					
Static VDD Supply Current I <sub>VDD_Stat</sub>	V <sub>IN</sub> =GND or VDD T <sub>C</sub> =85°C T <sub>C</sub> =230°C		17 22		μA
Static PVDD Supply Current I <sub>PVDD_Stat</sub>	V <sub>IN</sub> =GND or VDD T <sub>C</sub> =85°C T <sub>C</sub> =230°C		140 180		μA
<b>Input Signals</b>					
Input Low Voltage V <sub>IL</sub>	T <sub>C</sub> =85°C		1.7		V
Input High Voltage V <sub>IH</sub>	T <sub>C</sub> =85°C		3.3		V
Input Current I <sub>IN</sub>	V <sub>IN</sub> =GND or VDD T <sub>C</sub> =85°C T <sub>C</sub> =230°C		3.4 4.5		μA
<b>Under Voltage Lockout (UVLO) on PVDD to PGND (high-side)</b>					
V <sub>PVDD</sub> Start Voltage <sup>1</sup> V <sub>UVLOR</sub>	Rising VDD/PVDD threshold	3.2	3.5	3.8	V
V <sub>PVDD</sub> Start-stop Hysteresis V <sub>UVLOH</sub>			300		mV
<b>Output Transistors</b>					
Drain-Source Breakdown Voltage V <sub>(BR)DSS</sub>	T <sub>C</sub> =25°C	650			V
Maximum Continuous Drain-source Voltage V <sub>DS_Max</sub>		300			V
Off-State Drain Current I <sub>DSS</sub>	Output transistor OFF and V <sub>DS</sub> =300V T <sub>C</sub> =85°C T <sub>C</sub> =230°C		0.03 18	0.2 75	μA
Continuous Drain Current I <sub>D(DC)</sub>	T <sub>J</sub> =85°C T <sub>J</sub> =230°C		3.9 2.5		A
Static ON Resistance R <sub>DSon</sub>	I <sub>DRAIN</sub> =100mA T <sub>C</sub> =85°C T <sub>C</sub> =230°C		330 600	480 750	mΩ
<b>Source-Drain Body Diode</b>					
Continuous Forward Current I <sub>BD</sub>		1			A
Forward Voltage V <sub>BD</sub>	I <sub>Body</sub> =1A T <sub>C</sub> =85°C T <sub>C</sub> =230°C		0.99 1.00		V
<b>Bootstrap Diode</b>					
Continuous Forward Current I <sub>BSTD</sub>	V <sub>F</sub> =1.5V T <sub>C</sub> =85°C T <sub>C</sub> =230°C		0.52 0.50		A
Forward Voltage V <sub>BSTD</sub>	I <sub>BSTD</sub> =300mA T <sub>C</sub> =85°C T <sub>C</sub> =230°C		1.22 1.15		V

<sup>1</sup> Below this threshold the output nMOS is OFF, for PVDD rising.

## ELECTRICAL SPECIFICATIONS (CONTINUED)

### DYNAMIC CHARACTERISTICS

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, VDS=150V, IDRAIN=1A, -60°C<Tc<230°C.

Parameter	Condition	Min	Typ	Max	Units
<b>Supply Current</b>					
Dynamic VDD Supply Current $I_{VDD\_Dyn}$	For input Freq = 1MHZ and duty cycle=50% Tc=-60°C Tc=230°C		44 60		μA
Dynamic PVDD Supply Current $I_{PVDD\_Dyn}$	Freq=200kHz and duty cycle=50% Freq=1MHz and duty cycle=50%		2 10		mA
<b>Maximum drain current and DESAT protection</b>					
Peak Drain Current during Blanking Time $I_{Dpeak}$	250ns pulse Tc=-60°C Tc=230°C		15.3 8.3		A
Desaturation Drain Current after Blanking Time $I_{DESAT}$	Tc=-60°C Tc=85°C Tc=230°C		14.1 9.3 8.1		A
Blanking Time <sup>1</sup> $t_{Blank}$	Tc=-60°C Tc=85°C Tc=230°C		665 545 535		ns
Soft Turn-off Time $t_{SSD}$ <sup>2</sup>	Tc=-60°C Tc=85°C Tc=230°C		220 240 340		ns
<b>Switching Time</b>					
Delay ON Time <sup>3</sup> $t_{d(ON)}$	V <sub>DRAIN</sub> =20V, I <sub>DS</sub> =300mA Tc=-60°C Tc=230°C		120 220		ns
Delay OFF Time $t_{d(OFF)}$	Tc=-60°C Tc=230°C		160 290		ns

<sup>1</sup> Once output transistor is turned on, a comparator checks if  $I_{DS} < I_{DESAT}$  after this blanking time.

<sup>2</sup> If desaturation arises ( $I_{DS} > I_{DESAT}$ ) after the blanking time, the output transistor is softly turned OFF during the  $t_{SSD}$  time.

<sup>3</sup> From 10% input signal to 10% V<sub>DS</sub> on the output transistor.

## THEORY OF OPERATION

### Introduction

The XTR23012 implements a 300V cascode power transistor with integrated driver able to operate from -60°C to +230°C. Unique features of this product make it an extremely flexible block when designing power switching applications.

To ease adoption, the XTR23012 includes several protection features:

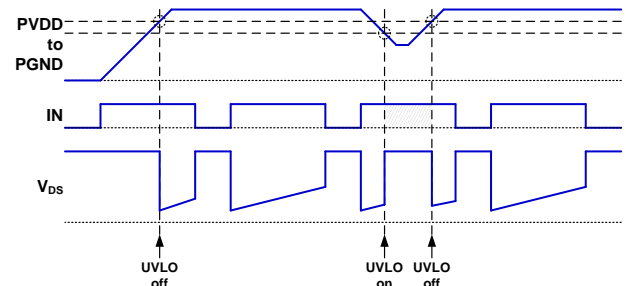
- Despite the recommended upper DC limit voltage on VDD and PVDD, the circuit can tolerate repetitive transient spike voltages up to 3V above the operation limits.
- Desaturation protection is implemented which softly turns off the output transistor whenever its current level exceeds a defined current threshold when in ON state (after a defined blanking time).
- Soft shut-down is implemented to prevent high dV/dt and di/dt on the application when the desaturation protection is activated.
- UVLO on the output stage guarantees the output transistor is off below a defined supply threshold.
- The recommended V<sub>DD</sub> range is between 4.5V and 5.5V. However, at lower V<sub>DD</sub>, the circuit could be functional as expected (with longer propagation delay). For very low V<sub>DD</sub> voltages (under 2-3V), it is guaranteed that the output transistor is off. Using this circuit below V<sub>DD</sub>=4.5V is however not recommended.

### Protections

#### Under Voltage Lockout (UVLO)

An UVLO detector continuously monitors the output stage supply voltage. During power-up, the UVLO protection guarantees that the output transistor is in off state below the V<sub>UVLOR</sub> threshold for whichever state of the input signals.

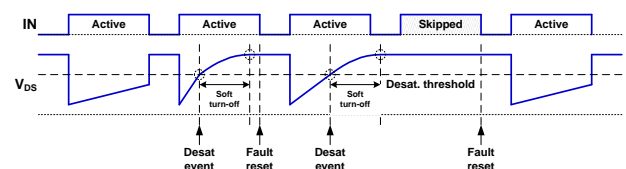
In case the UVLO protection is activated (UVLO on) while the output transistor is ON, this latter is immediately turned off. Once the UVLO event disappears (UVLO off), the output transistor state follows the input state.



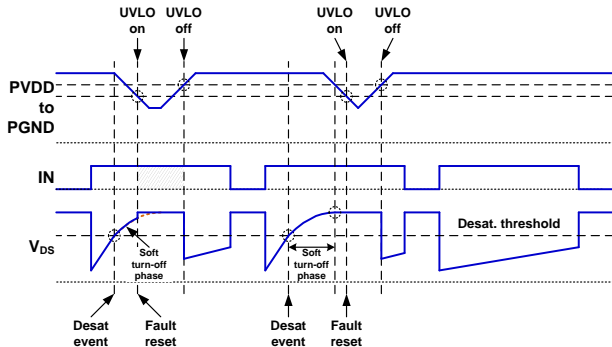
#### Desaturation (DESAT)

At each turn on of the output transistor, after a blanking time during which the desaturation protection is not allowed to react, the drain to source voltage of each output transistor is continuously compared to an internal voltage threshold. For V<sub>DS</sub> below this desaturation threshold, the output transistor still operates in its resistive regime.

If a desaturation event occurs after the blanking time, the output transistor is softly turned off and it remains off until the fault is cleared. If no UVLO event occurs during the soft shut down phase, the desaturation fault is cleared by the next falling edge of the corresponding input signal provided that the previous soft turn off is finished. If the soft shut down phase is not finished when the first falling edge arrives, the next input pulse is skipped and the output transistor remains off for one more period of the input signal.



If the UVLO is activated during a soft shut down phase, the UVLO protection takes over and immediately shuts down the output transistor. The activation of the UVLO protection also resets the desaturation fault, and the device can be turned on again as soon as the UVLO fault disappears.

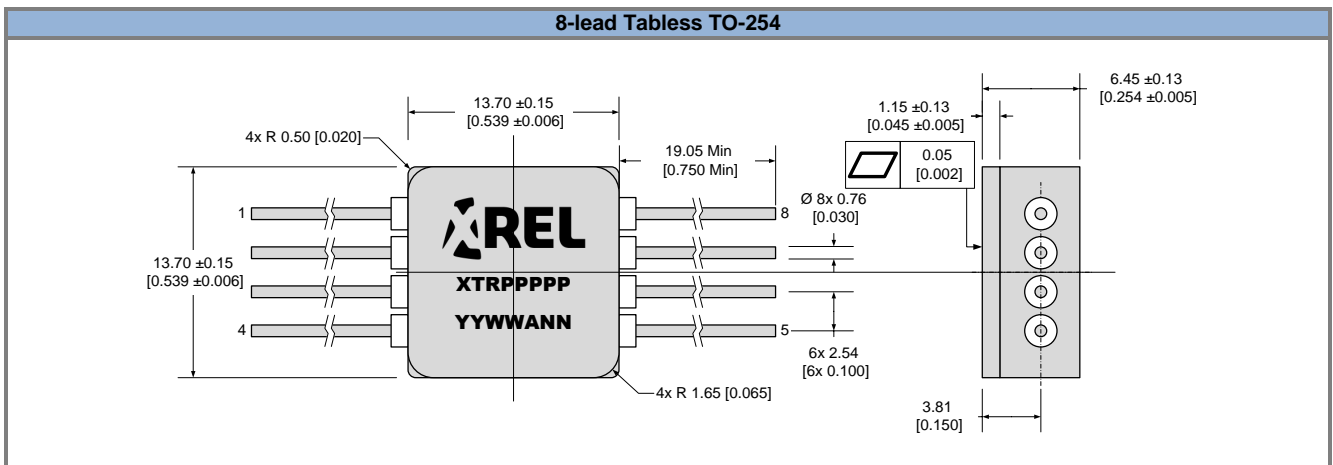


### Robustness against over voltages

Though it is highly recommended to comply with the DC voltage limits of the part, in switching applications it is usually difficult to guarantee that aggressive spikes cannot occur in some cases due to fast dV/dt and di/dt. For these reasons, the XTR23012 has been implemented in such a way that spikes of several volts over the recommended DC limits would not damage the device. For safe long term reliability, these spikes should however be reduced by correct PCB layout, ground planes and enough decoupling.

## PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances  $\pm 0.13$  mm [ $\pm 0.005$  in] unless otherwise stated.



### Part Marking Convention

<b>Part Reference: XTRPPPPPP</b>	
<b>XTR</b>	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
<b>PPPPPP</b>	Part number (0-9, A-Z).
<b>Unique Lot Assembly Code: YYWWANN</b>	
<b>YY</b>	Two last digits of assembly year (e.g. 15 = 2015).
<b>WW</b>	Assembly week (01 to 52).
<b>A</b>	Assembly location code.
<b>NN</b>	Assembly lot code (01 to 99).

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