HIGH-TEMPERATURE 40V HIGH AND LOW-SIDE N-CHANNEL POWER MOSFET WITH DRIVER

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Independent inputs for high-side and low-side switch.
- ▲ Standard Schmitt-trigger CMOS inputs.
- ▲ Plug-and-play with any digital 5V output.
- ▲ Over current (desaturation) protection with soft-shut-down on both switches.
- ▲ Under voltage lockout UVLO protection on output stages.
- ▲ Low on-resistance 330 mΩ @ 230°C.
- ▲ Large peak current capabilities 8.3A @ 230°C.
- ▲ Low On- and Off-time (220nsec and 290nsec @ 230°C).
- ▲ Latch-up free.
- ▲ Ruggedized 8-lead tablessTO254 package.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ DC/DC converters, motor drive, point-of-load power converters, power switching, PWM control.

DESCRIPTION

XTR21412 features an independent input high- and low-side N-channel MOSFETs with integrated driver. High- and low-side MOSFETs implement a totem-pole power stage suitable for power conversion applications up to 40V.

The inputs of the XTR21412 can be directly driven by any 5V digital output, making them fully plug-and-play devices, avoiding any time consuming optimization of the matching network between driver and power transistor.

XTR21412 parts are robust to usual spikes associated with parasitic inductors and fast transients in switching applications.

Functional features of XTR21412 include UVLO at the output stage and desaturation protection of each output transistor with soft shut-down functionality.

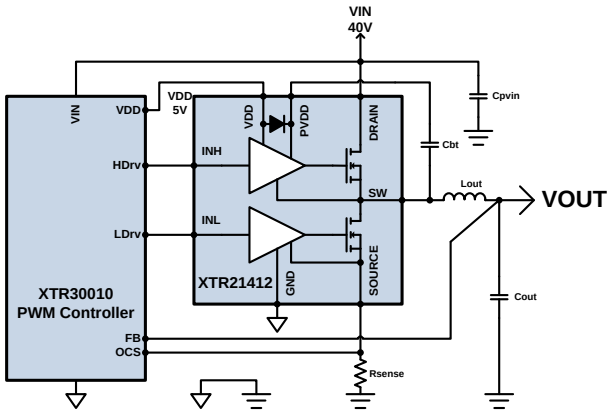
Full functionality is guaranteed from -60°C to +230°C, though operation well beyond this temperature range is achieved.

The XTR21412 has been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

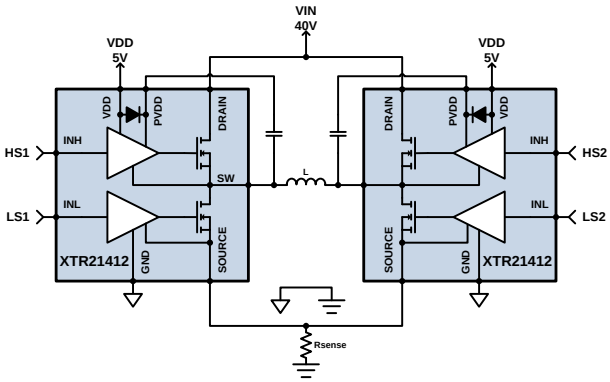
The XTR21412 is available in ruggedized 8-lead tabless TO254 packages. Ask X-REL Semiconductor for other packages and bare die availability.

PRODUCT HIGHLIGHT

Buck DC-DC Converter



Full-bridge Application



ORDERING INFORMATION

X	TR	21	412
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel ER = HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR21412-T	-60°C to +230°C	Tabless TO254	8	XTR21412

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply. Ask X-REL Semiconductor for bare die availability.

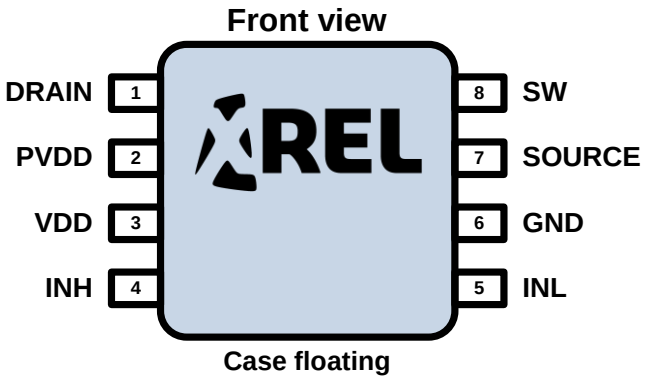
ABSOLUTE MAXIMUM RATINGS

Voltage on DRAIN to SOURCE	-1.5 to 55V
Voltage on DRAIN to SW and SW to SOURCE	-1.5 to 55V
Voltage on SW to GND	-1 to 55V
Voltage on INL, INH or VDD to GND	-0.5 to 6.0V
Voltage on PVDD to SW	-0.5 to 7.5V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

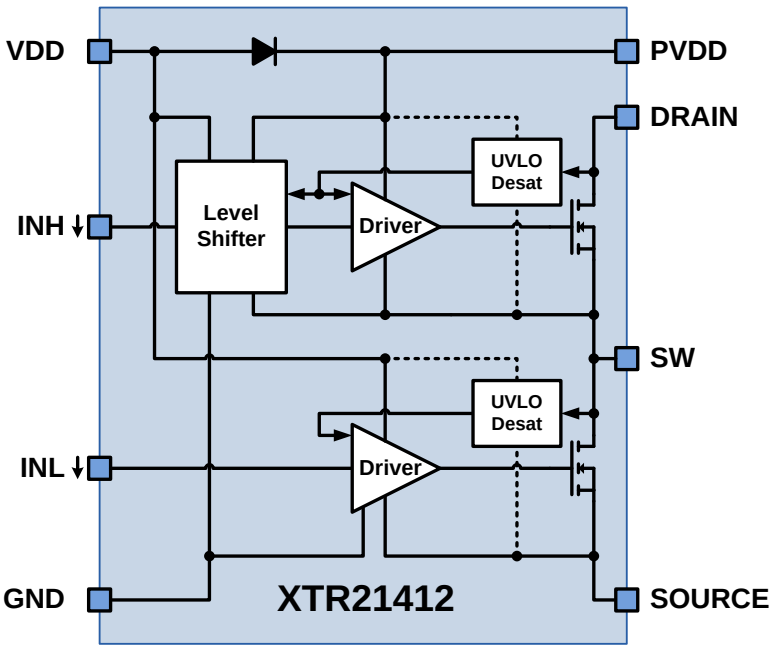
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PACKAGING

Tabless TO254



BLOCK DIAGRAM



Arrows aside pin names indicate whether the input is internally pulled up or down.

PIN DESCRIPTION

XTR21412-T		
Pin Number	**Name**	**Description**
1	**DRAIN**	Drain of the power NMOS transistor.
2	**PVDD**	Supply voltage of power section. Referenced to SOURCE.
3	**VDD**	Supply voltage of the input section. Referenced to GND.
4	**INH**	High-side input signal. Referenced to GND. Internally pulled down.
5	**INL**	Low-side input signal. Referenced to GND. Internally pulled down.
6	**GND**	Circuit ground.
7	**SOURCE**	Source of the power NMOS transistor.
8	**SW**	Switching node.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Power stage supply voltage **DRAIN** to **SOURCE**	0		40	V
Switching node voltage **DRAIN** to **SW** or **SW** to **SOURCE**	-1		40	V
Input stage supply voltage **VDD** to **GND**	4.5		5.5	V
High-side supply voltage **PVDD** to **SW**	See UVLO threshold		5.5	V
Low-side voltage to ground **SOURCE** to **GND**	-1.5		1	V
Input voltage **INL** or **INH** to **GND**	-0.3		VDD	V
Junction Temperature[1] T_j	-60		230	°C

[1] Operation beyond the specified temperature range is achieved with little degradation on electrical parameters.

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR21412-T (8-lead TO254)					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$			5		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$			45		°C/W

ELECTRICAL SPECIFICATIONS

STATIC CHARACTERISTICS

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD Supply Current **I_{VDD_Sta}**	V_{IN}=GND or VDD T_C=85°C T_C=230°C		180 240		µA
Static PVDD Supply Current **I_{PVDD_Sta}**	V_{IN}=GND or VDD T_C=85°C T_C=230°C		140 180		µA
Input Signals					
Input Low Voltage **V_{IL}**	T_C=85°C		1.7		V
Input High Voltage **V_{IH}**	T_C=85°C		3.3		V
Input Current **I_{IN}**	VIN=GND or VDD T_C=85°C T_C=230°C		3.4 4.5		µA
Under Voltage Lockout (UVLO): VDD (low-side), PVDD (high-side)					
V_{DD} or V_{PVDD} Start Voltage[1] **V_{UVLOR}**	Rising VDD/PVDD threshold	3.2	3.5	3.8	V
V_{DD} or V_{PVDD} Start-stop Hysteresis **V_{UVLOH}**			300		mV
Output Transistors					
Drain-Source Breakdown Voltage **$V_{(BR)DSS}$**	T_C=25°C	55V			V
Off-State Drain Current **I_{DSS}**	Output transistor OFF and V_{DS}=40V T_C=85°C T_C=230°C		0.03 18	0.2 75	µA
Continuous Drain Current **$I_{D(DC)}$**	T_J=85°C T_J=230°C		3.9 2.5		A
Static ON Resistance **R_{DSon}**	I_{DRAIN}=100mA T_C=85°C T_C=230°C		220 330		mΩ
Source-Drain Body Diode					
Continuous Forward Current **I_{BD}**		1			A
Forward Voltage **V_{BD}**	I_{Body}=1A T_C=85°C T_C=230°C		0.88 0.73		V
Bootstrap Diode					
Continuous Forward Current **I_{BSTD}**	V_F=1.5V T_C=85°C T_C=230°C		0.52 0.50		A
Forward Voltage **V_{BSTD}**	I_{BSTD}=300mA T_C=85°C T_C=230°C		1.22 1.15		V

[1] Below this threshold, the output nMOS is OFF, for VDD (low-side) or PVDD (high-side) rising.

ELECTRICAL SPECIFICATIONS (CONTINUED)

DYNAMIC CHARACTERISTICS

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Dynamic VDD Supply Current I_{VDD_Dyn}	INL and INH are driven be two non-overlaped, independent signals. Freq=200kHz and duty cycle=50% Freq=1MHz and duty cycle=50%		 2 10		 mA
Dynamic PVDD Supply Current I_{PVDD_Dyn}	INL and INH are driven be two non-overlaped, independent signals. Freq=200kHz and duty cycle=50% Freq=1MHz and duty cycle=50%		 2 10		 mA
Maximum drain current and DESAT protection					
Peak Drain Current during Blanking Time I_{Dpeak}	150ns pulse; V_{DS}=20V T_C=-60°C T_C=230°C		 15.3 8.3		 A
Desaturation Drain Current after Blanking time I_{DESAT}	T_C=-60°C T_C=85°C T_C=230°C		14.1 9.3 8.1		A
Blanking Time[1] t_{Blank}	T_C=-60°C Tc=85°C T_C=230°C		665 545 535		ns
Soft Turn-off Time t_{SSD}[2]	T_C=-60°C Tc=85°C T_C=230°C		220 240 340		ns
Switching Time					
Delay ON Time [3] $t_{d(ON)}$	V_{DRAIN}=20V, I_{DS}=300mA T_C=-60°C T_C=230°C		 120 220		 ns
Delay OFF Time $t_{d(OFF)}$	T_C=-60°C T_C=230°C		160 290		ns

[1] Once V_{GS} of the output transistor is high, a comparator checks if I_{DS}<I_{DESAT} after this blanking time.
[2] If desaturation arises (I_{DS}>I_{DESAT}) after the blanking time, the output transistor is softly turned OFF during the t_{SSD} time.
[3] From 10% input signal to 10% V_{DS} on the output transistor.

THEORY OF OPERATION

Introduction

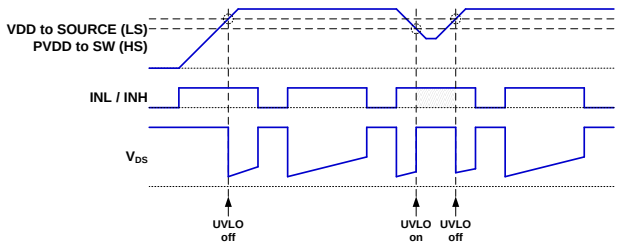
The XTR21412 implements a 40V totem-pole output stage made of two N-channel MOS transistors with integrated driver able to operate from -60°C to +230°C. Unique features of this product make it an extremely flexible block when designing power switching applications.
To ease adoption, the XTR21412 includes a high-current bootstrap diode from VDD to PVDD (output stage) as well as several protection features:

- Despite the recommended upper DC limit voltage on VDD and PVDD, the circuit can tolerate repetitive transient spike voltages up to 3V above the operation limits.
- Desaturation protection is implemented which softly turns off the output transistor whenever its current level exceeds a defined current threshold when in ON state (after a defined blanking time).
- Soft shut-down is implemented to prevent high dV/dt and di/dt on the application when the desaturation protection is activated.
- UVLO on the output stage of each power switch guarantees the output MOSFET is off bellow a defined supply threshold.
- The recommended V_{DD} range is between 4.5V and 5.5V. However, at lower V_{DD}, the circuit could be functional as expected (with longer propagation delay). For very low V_{DD} voltages (under 2-3V), it is guaranteed that the output MOSFET is off. Using this circuit bellow V_{DD}=4.5V is however not recommended.

Protections

Under Voltage Lockout (UVLO)

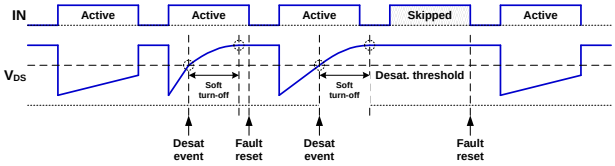
An UVLO detector continuously monitors the output stage supply voltage. During power-up, the UVLO protection guarantees that the output transistor is in off state below the V_{UVLOR} threshold for whichever state of the input signals.
In case the UVLO protection is activated (UVLO on) while the output transistor is ON, this latter is immediately turned off. Once the UVLO event disappears (UVLO off), the output transistor state follows the input state.



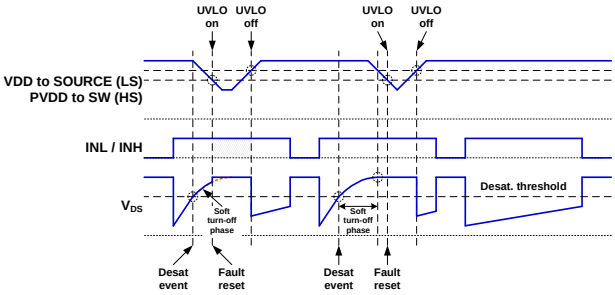
Desaturation (DESAT)

At each turn on of the output transistor, after a blanking time during which the desaturation protection is not allowed to react, the drain to source voltage of each output transistor is continuously compared to an internal voltage threshold. For V_{DS} below this desaturation threshold, the output transistor still operates in its resistive regime.
If a desaturation event occurs after the blanking time, the output transistor is softly turned off and it remains off until the fault is cleared. If no UVLO event occurs during the soft shut down phase, the desaturation fault is cleared by the next falling edge of the corresponding input signal provided that the previous soft turn off is finished. If the soft shut down phase is not finished when the first falling edge arrives, the next input pulse is skipped

and the output transistor remains off for one more period of the input signal.



If the UVLO is activated during a soft shut down phase, the UVLO protection takes over and immediately shuts down the output transistor. The activation of the UVLO protection also resets the desaturation fault, and the device can be turned on again as soon as the UVLO fault disappears.



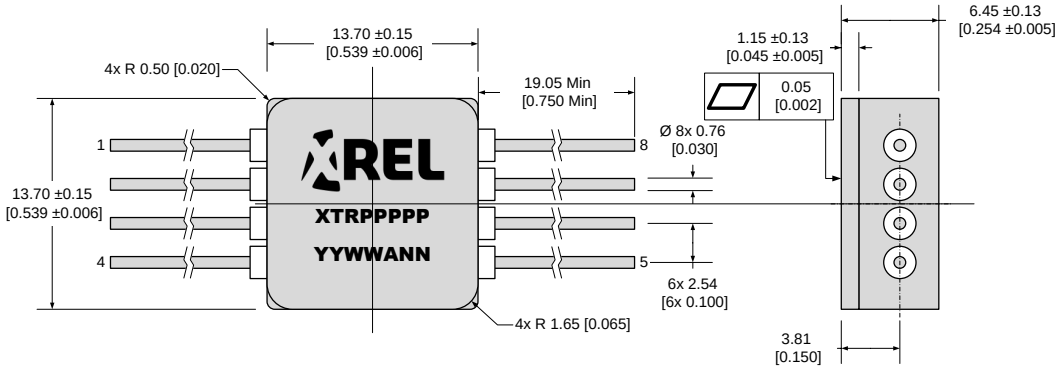
Robustness against over voltages

Though it is highly recommended to comply with the DC voltage limits of the part, in switching applications it is usually difficult to guarantee that aggressive spikes cannot occur in some cases due to fast dV/dt and di/dt. For these reasons, the XTR21412 has been implemented in such a way that spikes of several volts over the recommended DC limits would not damage the device. For safe long term reliability, these spikes should however be reduced by correct PCB layout, ground planes and enough de-coupling.

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise stated.

8-lead Tabless TO-254



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 15 = 2015).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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